

What is claimed is:

- 1 1. A computerized method for identifying structural regularity in a logic design, the
2 method comprising:
 - 3 receiving a plurality of templates covering the logic design;
 - 4 receiving one or more control signals for the logic design;
 - 5 receiving one or more databus identifiers for the logic design; and
 - 6 generating a first vector for the logic design through computer automated
7 operations to combine at least one instance of one of the plurality of templates based
8 on the control signals, the databus identifiers and connectivity of the logic design.
- 1 2. The computerized method of claim 1 wherein the first vector comprises each one
2 of the instances of a first one of the templates having a same set of the control signals
3 and feeding a same databus.
- 1 3. The computerized method of claim 2 wherein a second vector is generated from
2 each one of the instances of a second one of the templates having a same set of
3 connections in the logic design.
- 1 4. The computerized method of claim 1 wherein the plurality of templates is
2 received in a net list.
- 1 5. The computerized method of claim 1 wherein at least one of the plurality of
2 templates is a tree template.
- 1 6. The computerized method of claim 1 wherein at least one of the plurality of
2 templates is a multi-output template.
- 1 7. The computerized method of claim 1 wherein at least one of the plurality of
2 templates is a single-principal output template.
- 1 8. A computerized method for generating a set of vectors for a logic design through
2 computer-automated operations, the method comprising:
 - 3 identifying logic for generating at least one control signal and excluding the
4 logic from the set of vectors;
 - 5 identifying at least one instance of a first template to group as a first vector in

6 the set of vectors by using databus identifiers and the control signals; and
7 identifying at least one instance of a second template to group as a second
8 vector in the set of vectors by using circuit connectivity and a previously formed
9 vector.

1 9. The computerized method of claim 8, wherein identifying at least one instance of
2 the second template using circuit connectivity and a previously formed vector is
3 performed after all possible vectors are identified using the databus identifiers and
4 the control signals.

1 10. The computerized method of claim 8 wherein the logic design is for a datapath
2 circuit.

1 11. A computerized method of generating a layout for a logic design using vectors,
2 the method comprising:
3 receiving one or more vectors for the logic design;
4 receiving connectivity data for the logic design; and
5 generating a one-dimensional circuit layout for the logic design through
6 computer automated operations using the vectors and the connectivity data.

1 12. The computerized method of claim 11 wherein generating the one-dimensional
2 layout further comprises:
3 enumerating a plurality of solutions for the layout;
4 calculating a total wire length for each one of the solutions; and
5 selecting the solution with a minimum wire length.

1 13. The computerized method of claim 11 further comprising receiving critical path
2 data for the logic design.

1 14. The computerized method of claim 13 wherein generating the one-dimensional
2 layout further comprises:
3 enumerating a plurality of solutions for the layout;
4 calculating a cost for each one of the solutions; and
5 selecting the solution with a minimum cost for the critical path.

- 1 15. The computerized method of claim 11 wherein each one of the vectors forms a
2 row in the one-dimensional circuit layout.
- 1 16. The computerized method of claim 11 wherein the logic design is for a datapath
2 circuit.
- 1 17. A machine-readable media having machine-executable components
2 comprising:
3 a functional regularity extraction component to generate a plurality of
4 templates to cover a logic design;
5 a structural regularity extraction component to generate a set of vectors from
6 the plurality of templates; and
7 a floorplanning component to generate a circuit layout from the set of
8 vectors.
- 1 18. The machine-readable media of claim 17, wherein a vector in the set of vectors
2 is a group of template instances that are identical in function and structure.
- 1 19. The machine-readable media of claim 17 wherein the structural regularity
2 extraction component further comprises:
3 a control logic identifying component to identify logic for generating at least
4 one control signal and excluding the logic from the set of vectors;
5 a first vector identifying component to identify at least one instance of a first
6 template to group as a first vector in the set of vectors by using databus identifiers
7 and the control signals; and
8 a second vector identifying component to identify at least one instance of a
9 second template to group as a second vector in the set of vectors by using circuit
10 connectivity and a previously formed vector.
- 1 20. An article comprising:
2 a machine-readable media including instructions that when executed cause a
3 computer to:
4 receive a plurality of templates covering the logic design;
5 receive one or more control signals for the logic design;
6 receive one or more databus identifiers for the logic design; and
7 generate a first vector for the logic design through computer automated

8 operations to combine at least one of the plurality of templates based on the control
9 signals, the databus identifiers and connectivity of the logic design.

1 21. The article of claim 20 wherein the first vector comprises each one of the
2 instances of a first one of the templates having a same set of control signals and
3 feeding a same databus.

1 22. The article of claim 21 wherein a second vector is generated from each one of
2 the instances of a second one of the templates having a same set of connections in
3 the logic design.

1 23. An article comprising:

2 a machine-readable media including instructions that when executed cause a
3 computer to:

4 identify logic for generating at least one control signal and excluding the
5 logic from the set of vectors;

6 identifying at least one instance of a first template to group as a first vector in
7 the set of vectors by using databus identifiers and the control signals; and

8 identifying at least one instance of a second template to group as a second
9 vector in the set of vectors by using circuit connectivity and a previously formed
10 vector.

1 24. The article of claim 23, wherein identifying at least one instance of a second
2 template using circuit connectivity and a previously formed vector is performed after
3 all vectors are identified using the databus identifiers and the control signals.

1 25. An article comprising:

2 a machine-readable media including structural regularity extraction
3 instructions that when executed cause a computer to generate a set of vectors from a
4 plurality of templates.

1 26. An article comprising:

2 a machine-readable media including floorplanning instructions that when
3 executed cause a computer to generate a circuit layout from a set of vectors.
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